REMARKS

Claims 1, 3-47 are pending in this application. Claims 9-39 have been withdrawn from consideration. Claims 1 and 41 have been amended and claim 2 has been cancelled herein without prejudice or disclaimer.

Claim Rejections – 35 U.S.C. § 103

Claims 1-5, 7, 8, 40-44, 46 and 47 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahn *et al.* (U.S. Patent No. 6,586,792) in view of Campbell, The Science and Engineering of Microelectronic Fabrication, pages 29-31. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 has been amended to further recite "said Si oxide film having a surface state density of $10^{11}eV^{-1}cm^{-2}$ or less."

The Examiner concedes that Ahn *et al.* does not teach a silicon substrate comprising (111) oriented crystals. The Office Action contends, however, that Campbell teaches a silicon wafer formed of a boule and having a (111) orientation and thus it would have been obvious to one of ordinary skill in the art to select a commercially available wafer with a (111) orientation since it is commonly used in the art for p-type and n-type wafers.

In response to Applicants' arguments filed November 26, 2003, the Examiner contends that the motivation and suggestion to combine references is in the knowledge generally available to one of ordinary skill in the art. Specifically, the Examiner contends that it is desirable to form devices on wafers with a (111) surface because of the large density as would be appreciated by one of ordinary skill in the art. Applicants respectfully disagree.

Campbell discloses both a (111) and a (100) silicon crystal. Nowhere does the reference suggest that an insulation film can be formed on a (111) surface of the Si crystal. In addition, as conceded in the Office Action, Ahn *et al.* does not suggest that the gate insulation layer comprising silicon dioxide is formed on a (111) surface of an Si substrate. Moreover, neither Ahn *et al.* or Campbell disclose or suggest that it is desirable to form devices on wafers with a (111) surface because of the large density of the (111) surface. Furthermore, neither Ahn *et al.* or Campbell disclose or suggest that the Si oxide film which is formed on the Si crystal having a (111) surface has a surface state density of $10^{11}eV^{-1}cm^{-2}$ or less. Applicants respectfully submit that, for example, Figure 5 of the present application clearly shows that a surface state density of a thermal oxide film formed on a (111) surface of

Si is ten times larger than the surface state density of a thermal oxide film formed on the (100) surface of Si. From this result, one skilled in the art would expect that a silicon oxide film formed by a high-density Kr plasma on a (111) surface of Si would also have a surface state density more than ten times larger than a surface state density of a silicon oxide film formed on a (100) surface. However, contrary to what one ordinary skill in the art would expect, the invention of claim 1, achieves a silicon oxide film with a surface state density equal or less than $10^{11}eV^{-1}cm^{-2}$ even when the silicon oxide is formed on a (111) surface of Si.

In addition, there is no motivation in either Ahn *et al.* or Campbell to form a silicon dioxide film containing Kr on a (111) surface of a silicon crystal. The mere fact that Ahn *et al.* forms a gate oxide in high density krypton plasma at low temperature is not an indication that Ahn *et al.* forms a silicon dioxide film containing Kr on a (111) surface of a silicon crystal.

Applicants respectfully submit that prior to the present invention, no known process enabled formation of a high-quality high-dielectric film having an excellent electric property on a (111) surface of a Si crystal at low temperature. Furthermore, Applicants respectfully submit that prior to the present invention, no known process enabled formation of a silicon oxide film on a (111) surface of a Si crystal in which a surface state density of the silicon oxide film is equal or less than $10^{11}eV^{-1}cm^{-2}$.

Furthermore, contrary to Examiner's assertion, the knowledge that it is desirable to form devices on wafers with a (111) surface is not generally available to one of ordinary skill in the art. Indeed, the Examiner did not provide any evidence or reference supporting this assertion. In addition, as stated above, one ordinary skilled in the art would expect that a silicon oxide film formed by a high-density Kr plasma on a (111) surface of Si would have a surface state density more than ten times larger than a surface state density of a silicon oxide film formed on a (100) surface. As a result, there would be no motivation to one of ordinary skill in the art to form a silicon oxide film on a (111) surface of a silicon crystal.

Consequently, neither Ahn *et al.* nor Campbell, alone or in combination, disclose, teach or suggest the subject matter recited in claim 1.

With regard to claim 3, neither Ahn *et al.* nor Campbell teach or suggest an insulation film formed on a (111) surface of a Si crystal and a part of the insulation film comprises a Si oxide film and the silicon oxide formed on a (111) surface of a silicon crystal has a surface state density equal or less than $10^{11}eV^{-1}cm^{-2}$, much less that the part of the insulation film

comprises a Si oxide film containing Kr and that the Kr concentration level decreases in the Si oxide film from a surface of the Si oxide film to an interface between the Si oxide film and the Si crystal. In response to the argument filed November 26, 2003, the Examiner states that the Ahn *et al.* inherently teaches this feature since the process of forming the oxide is identical to that of the claimed invention.

The Examiner inference that the method of forming silicon dioxide of Ahn *et al.* would have inherently resulted in a Kr concentration that decreases from a surface of the silicon dioxide to an interface between the oxide and the crystal is based solely on the Examiner's assumption. There is no indication or suggestion in Ahn *et al.* that the Kr concentration would decrease in the manner recited in claim 3.

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).* In this case, the mere possibility that the Kr concentration may decrease from a surface of the silicon dioxide to an interface between the oxide in Ahn *et al.* because the process of forming the oxide in Ahn *et al.*, according to the Examiner, is identical to that of the claimed invention is not sufficient to establish obviousness. Applicants submit that the Examiner did not take into account the fact that claim 3 also recites, *inter-alia*, that the insulation film is formed on the (111) surface of the Si crystal.

Consequently, neither Ahn *et al.* nor Campbell, alone or in combination, disclose, teach or suggest the subject matter recited in claim 3.

With regard to claim 40, the Examiner's contention that Ahn *et al.* inherently teach that the silicon oxide film containing Kr reduces current leakage and improves breakdown characteristics of the insulation film when formed on a (111) surface is clearly improper. Simply, there is no suggestion in Ahn *et al.* that the insulation film can be formed on a (111) surface. Indeed, the current leakage is reduced and the breakdown characteristics are improved by forming the insulation film containing Kr on a (111) surface of a Si crystal. Since Ahn *et al.* does not teach anywhere forming an oxide film on a (111) surface of an Si crystal, Applicants respectfully submit that the argument of inherency cannot be ascertained and thus *prima facie* case of obviousness cannot be established.

Consequently, neither Ahn *et al.* nor Campbell, alone or in combination, disclose, teach or suggest the subject matter recited in claim 40.

Furthermore, with regard to claims 5 and 44, contrary to the Examiner's contention, the gate layer 20, in Ahn *et al.*, is simply deposited on weak-ferroelectric layer 18 and not on the gate insulation layer (silicon dioxide layer) 14. In response to Applicants' arguments, the Examiner contends that the gate layer is deposited on the gate insulation layer albeit there are intervening layers.

Claims 5 and 44 recite, *inter-alia*, " a gate electrode on said Si oxide film." According to a definition of a dictionary the preposition "on" is *used to indicate position above and supported by or in contact with: The vase is on the table.*[1] Therefore, according to this dictionary definition, a gate electrode on the Si oxide film means a gate electrode in contact with and on the Si oxide film. As there are intervening layers between the gate layer 20 and the gate insulation layer 14 in Ahn *et al.*, the gate layer in not "on" the gate insulation layer.

Therefore Applicants respectfully submit that claims 1, 3 and 40 are patentable and respectfully request that the rejection of claims 1, 3 and 40 under § 103(a) be withdrawn.

Claims 2, 4, 5, 7, 8, 41-44, 46 and 47 depend from either claim 1 or claim 40. Therefore, for at least the reasons presented above with regard to claims 1 and 40, claims 2, 4, 5, 7, 8, 41-44, 46 and 47 are patentable.

Therefore, Applicants respectfully request that the rejection of claims 2, 4, 5, 7, 8, 41-44, 46 and 47 under § 103(a) be withdrawn.

Claims 6 and 45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahn *et al.* (US Pat. No. 6,586,792) in view of Campbell, The Science and Engineering of Microelectronic Fabrication, pages 29-31 and further in view of Campbell, pages 394-396. Applicants respectfully traverse this rejection for at least the following reasons.

Claims 6 and 45 depend from either claim 1 or claim 40. Therefore, for at least the reasons provided above with regard to claim 1 and claim 40, claims 6 and 46 are patentable.

Furthermore, the Examiner concedes that Ahn *et al.* does not teach a semiconductor device wherein the crystal surface is part of a device isolation groove.

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[1]Excerpted from *The American Heritage Dictionary of the English Language, Third Edition*

The Examiner contends that it would have been obvious to incorporate the teachings of Campbell into the device of [Jacob *et al.*] (sic) Ahn *et al.* because Campbell teaches a trench isolation structure that is suitable for integrated circuits. However, as stated above neither Ahn *et al.* nor Campbell, alone or in combination, disclose, teach or suggest forming an insulation film on a (111) surface of the Si crystal. Even if the Si crystal of Campbell may include a trench, there is no suggestion in either Ahn *et al.* or Campbell that an insulation layer including a silicon oxide film containing Kr can be formed on a (111) surface of the Si crystal.

Therefore, Applicants respectfully request that the rejection of claim 6 and 46 under § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, the claims are now in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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